WHAT IS CLAIMED IS:

1. A random access memory device assembled into a chip package and including a refresh request control circuit, the refresh request control circuit comprising:

a first circuit configured to receive a first refresh rate signal having a first refresh rate signal frequency and configured to produce a second refresh rate signal having a second refresh rate signal frequency;

a second circuit configured to receive the first refresh rate signal and the second refresh rate signal; and

a final fusing element coupled to the second circuit such that the final fusing element selects a final refresh rate signal, the selection of the final refresh rate signal occurring after the dynamic memory storage system has been assembled into a chip package.

2. The random access memory device of claim 1 including a multitude of memory cells that must be periodically refreshed in order to retain data, the final refresh rate signal having a final refresh rate signal frequency that is sufficient to refresh the memory cells often enough to retain data.

3. The random access memory device of claim 2 wherein the final refresh rate signal is selected from the first and second refresh rate signals.

4. The random access memory device of claim 3 wherein second refresh rate that is different than, and a derivative of, the first refresh rate frequency

5. The random access memory device of claim 1 further comprising:

a third circuit configured to produce multiple interim signals of varying frequencies;

a fourth circuit configured to receive the multiple interim signals of varying frequencies; and

an initial fusing element coupled to the fourth circuit such that the initial fusing element selects the first refresh rate signal from the multiple interim signals of varying frequencies.

6. The random access memory device of claim 5 wherein the initial fusing element selects the first refresh rate signal by laser cutting a fuse in the initial fusing element while the random access memory device is at a wafer level of processing.

7. The random access memory device of claim 5 wherein the initial fusing element selects the first refresh rate signal by electronically cutting a fuse in the initial fusing element.

8. The random access memory device of claim 5 wherein third circuit is a frequency divider and the fourth circuit is a multiplexer.

9. The random access memory device of claim 1 wherein the final fusing element selects the final refresh rate signal by electronically cutting a fuse in the final fusing element after random access memory device is assembled into a chip package.

10. A refresh request control circuit for use in a random access memory device assembled into a chip package and having a multitude of memory cells that must be periodically refreshed in order to retain data, the refresh request control circuit comprising:

a signal generator that produces an oscillating signal;

a first frequency divider configured to receive the oscillating signal from the first frequency divider and to produce multiple output signals, each having a different frequency;

a first multiplexer configured to receive the multiple output signals from the first frequency divider;

a first fusing element coupled to the first multiplexer such that the first fusing element selects a first refresh rate signal from the multiple output signals, the first refresh rate signal having a first refresh rate signal frequency;

a second frequency divider configured to receive the first refresh rate signal from the first multiplexer and to produce a second refresh rate signal having a second refresh rate signal frequency that is different than the first refresh rate signal frequency;

a second multiplexer configured to receive the first and second refresh rate signals; and

a second fusing element coupled to the second multiplexer such that the second fusing element selects a final refresh rate signal, the selection occurring after the random access memory device has been assembled into a chip package.

11. The random access memory device of claim 10 wherein the final refresh rate signal has a signal frequency that is sufficient to refresh the memory cells often enough to retain data in the random access memory device.

12. The random access memory device of claim 10 wherein the first fusing element selects the first refresh rate signal by laser cutting the first fusing element while the random access memory device is at a wafer level.

13. A method of setting the refresh signal rate for periodically refreshing memory cells in a random access memory device that is assembled into a chip package, the method including the steps of:

providing a random access memory device with a multitude of memory cells and a refresh rate control circuit;

initially programming the refresh rate control circuit such that it generates a first refresh rate signal with an first refresh rate signal frequency;

determining whether the first refresh rate signal frequency is sufficient to retain data in the memory cells of the random access memory device;

providing a second refresh rate signal having a second refresh rate signal frequency; and

after the random access memory device is assembled into a chip package, further programming the refresh rate control circuit to select a final refresh rate signal based on the determination of whether the first refresh rate signal frequency is sufficient to retain data in the memory cells.

14. The method of claim 13 further including receiving the first and second refresh rate signals with a multiplexer that can be controlled to select the final refresh rate signal for output from the multiplexer to be used in refreshing the memory cells of the random access memory device.

15. The method of claim 14 wherein the step of further programming the refresh rate control circuit to provide the final refresh rate signal includes cutting or leaving uncut a fusing element, which is coupled to the multiplexer such that the fusing element controls the multiplexer and the selection of the final refresh rate signal.

16. The method of claim 13 wherein the step of determining whether the first refresh rate signal frequency is sufficient to retain data in the memory cells of the random access memory device occurs after the random access memory device is packaged into a chip.

17. A random access memory device assembled into a chip package and including a refresh request control circuit, the refresh request control circuit comprising:

first means for receiving a first refresh rate signal having a first refresh rate signal frequency and for producing a second refresh rate signal having a second refresh rate signal frequency; and

second means for receiving the first refresh rate signal and the second refresh rate signal and for selecting a final refresh rate signal after the random access memory device has been assembled into a chip package.

18. The random access memory device of claim 17 wherein first means includes a frequency divider.

19. The random access memory device of claim 17 wherein second means includes a multiplexer and a fusing element, the multiplexer configured to receive the first and second refresh rate signals.

20. The random access memory device of claim 18 wherein the fusing element controls the multiplexer in order to select the final refresh rate signal after the random access memory device has been assembled into a chip package.